FIG. 1A

DYNAMICALLY ADJUSTABLE DIGITAL GYRATOR HAVING EXTENDED FEEDBACK

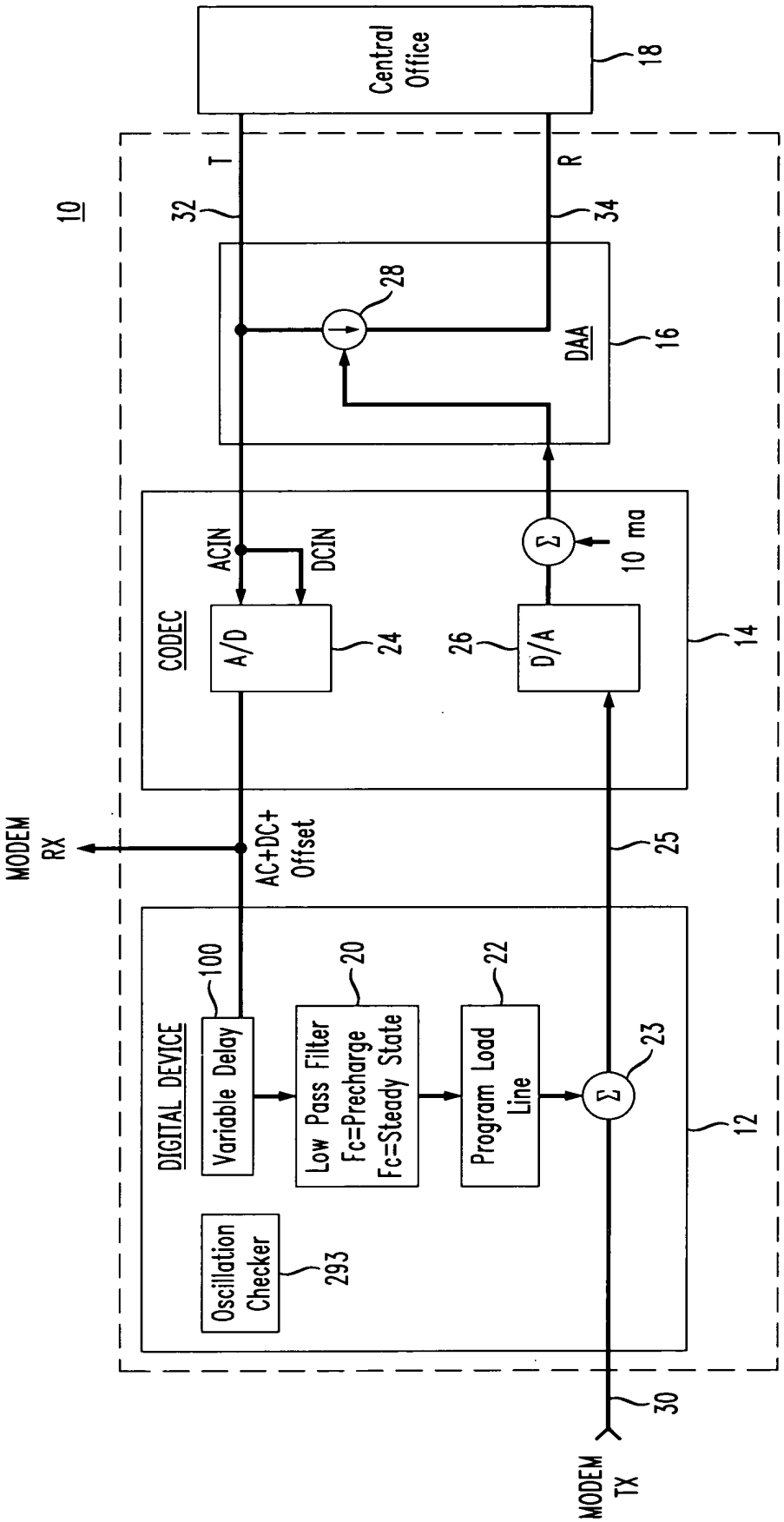


FIG. 1B

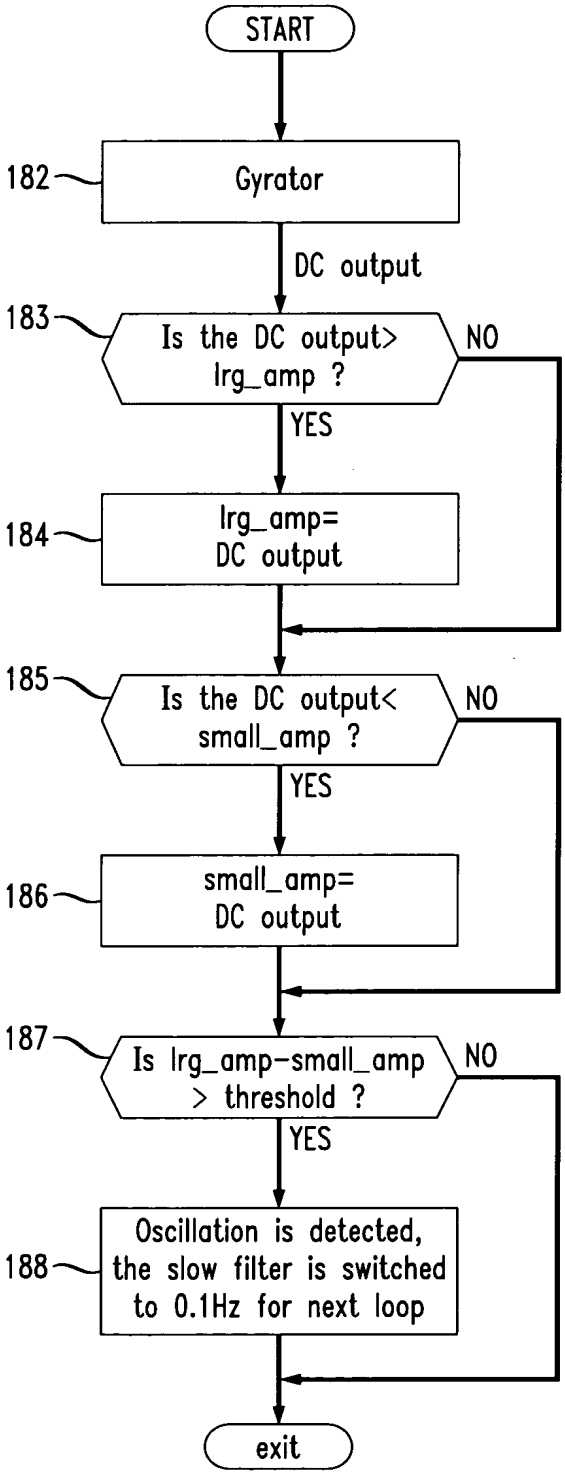
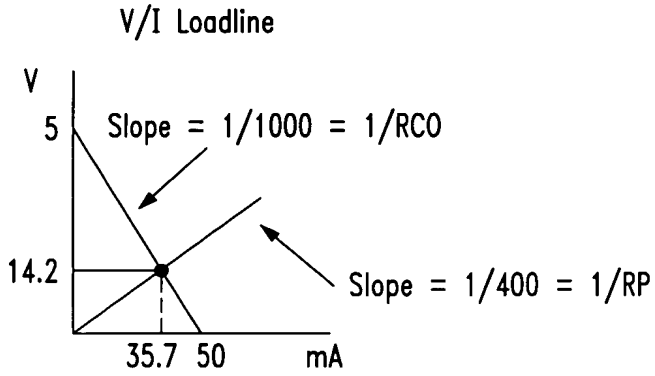


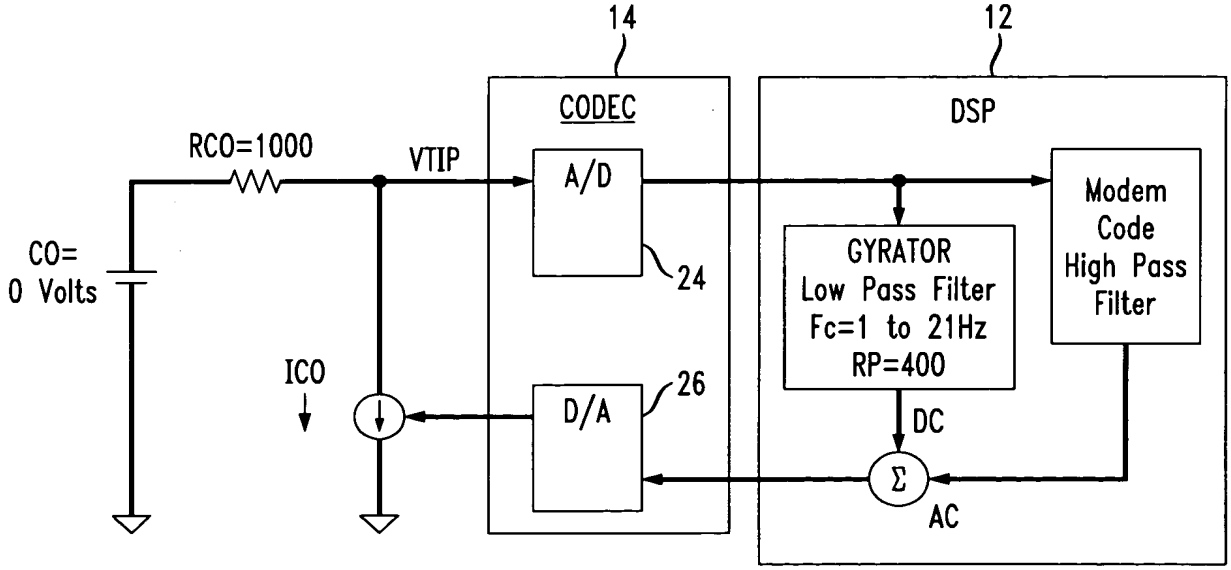
FIG. 2A



50-ICO*RCO=ICO*RP=VP
ICO=14.27 mA
VP=35.7 Volts
Note: All results are at steady state

FIG. 2B

DYNAMICALLY ADJUSTABLE DIGITAL GYRATOR EXAMPLE



RP=Gyrator Impedance=400 ohms
RCO=Central Office Resistance

FIG. 3A

CODEC and Telephone System Stability Block Diagram

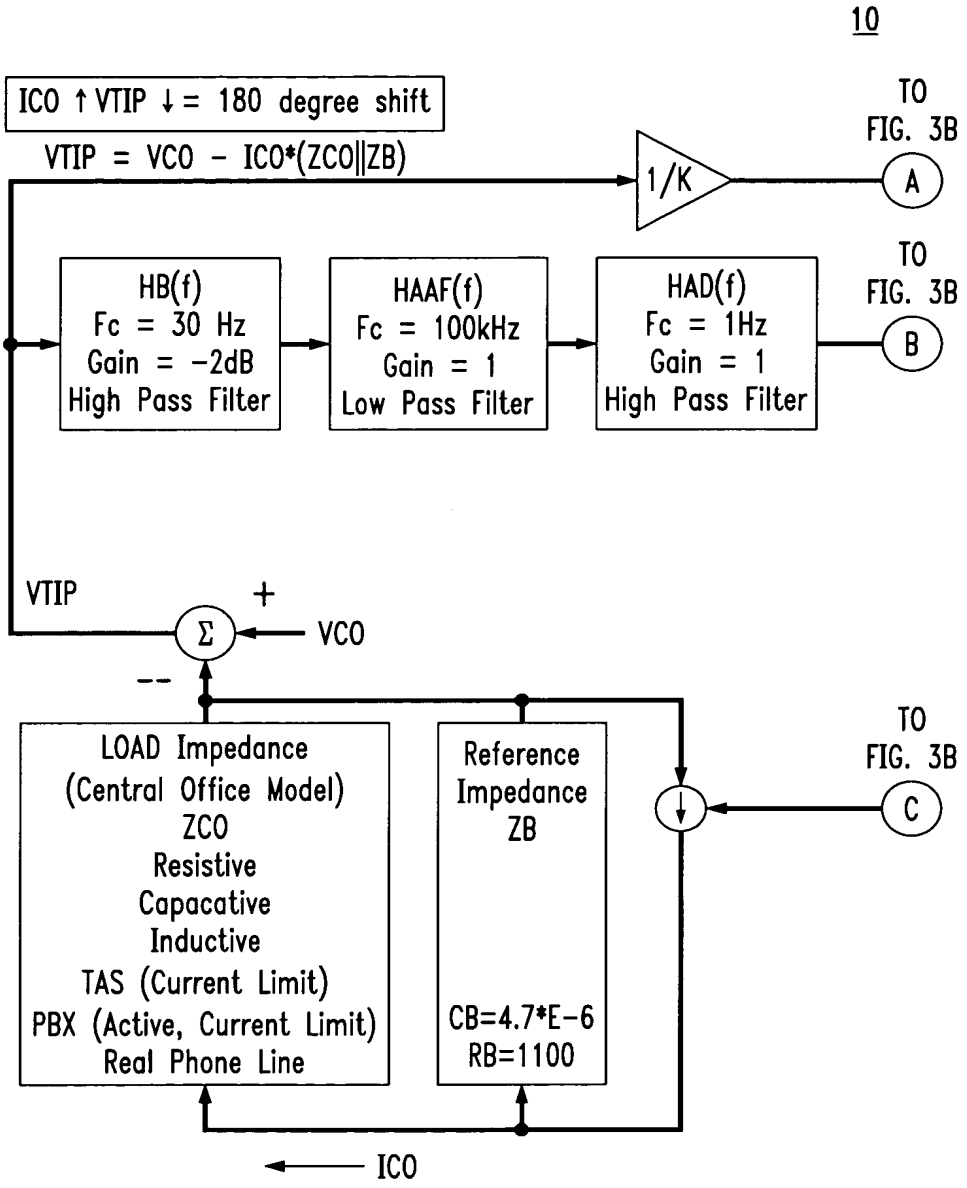


FIG. 3B

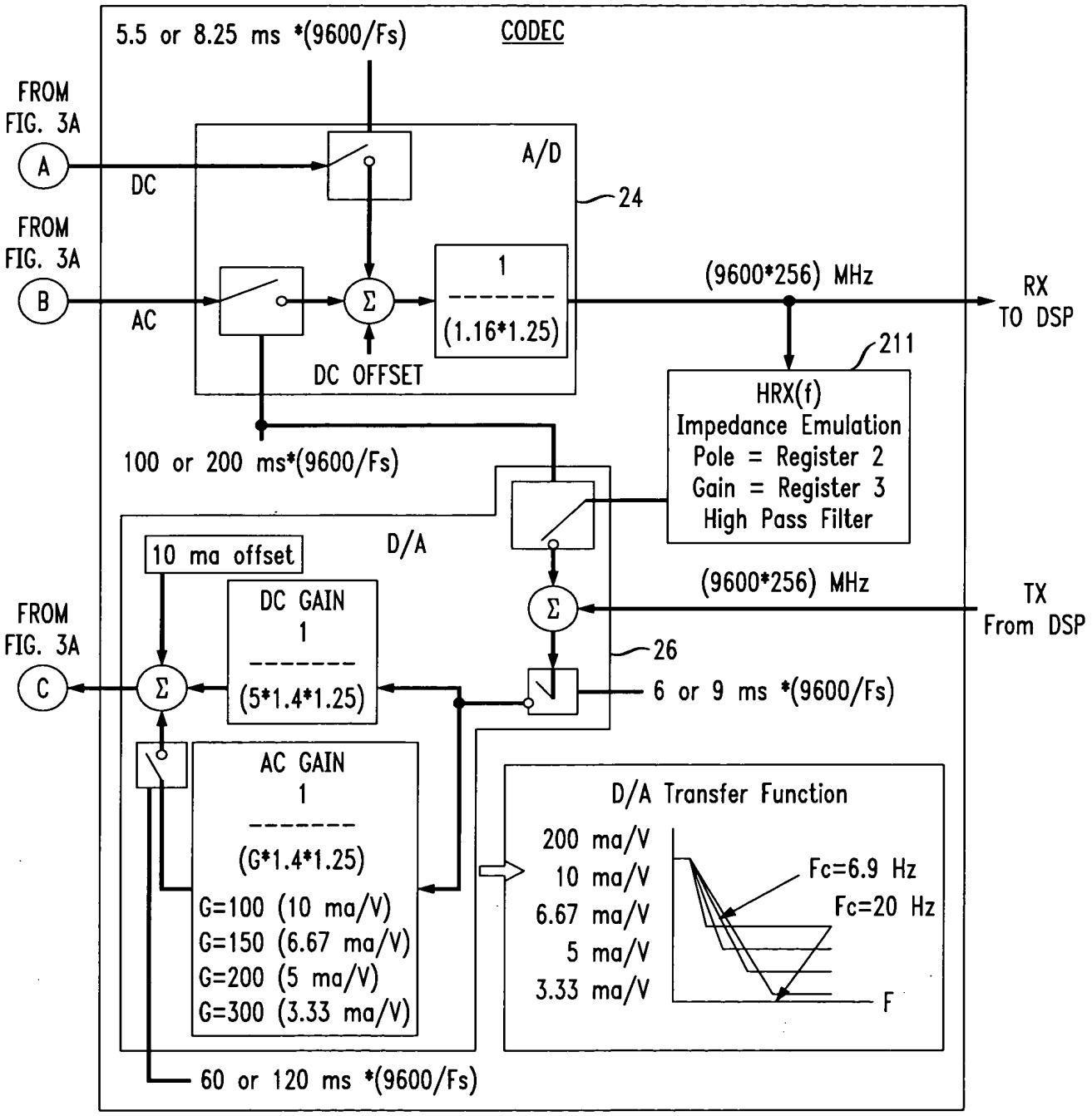


FIG. 4

Simplified D/A Path

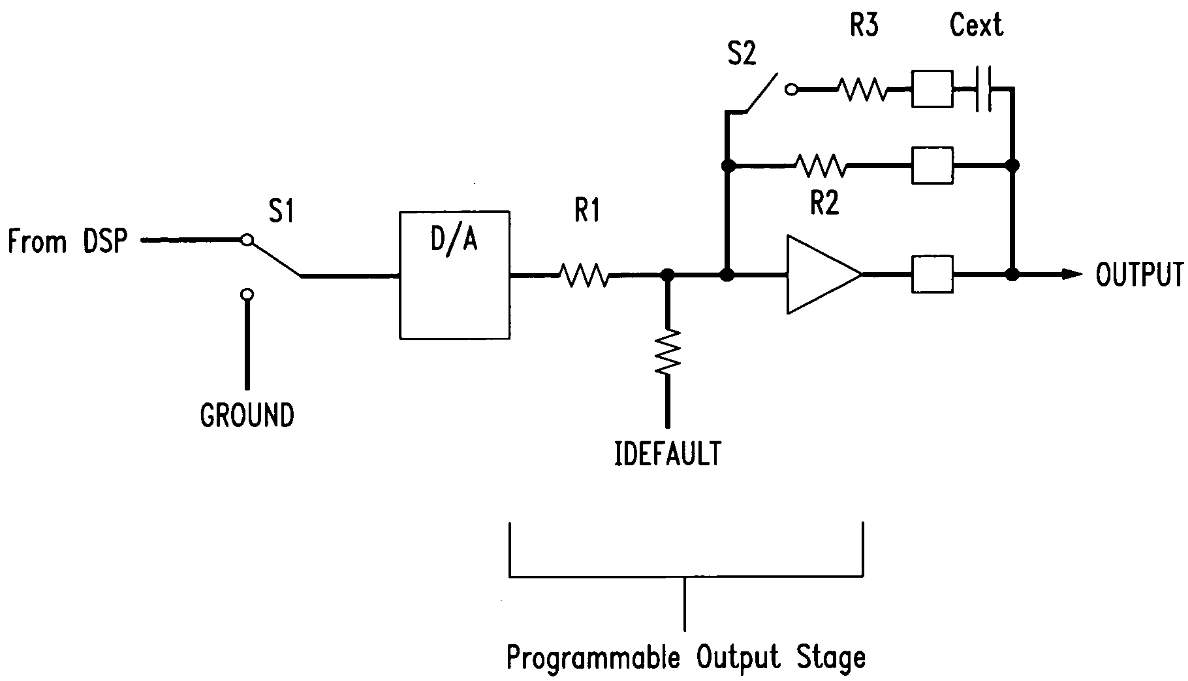


FIG. 5A

DSP Based Gyrator Block Diagram

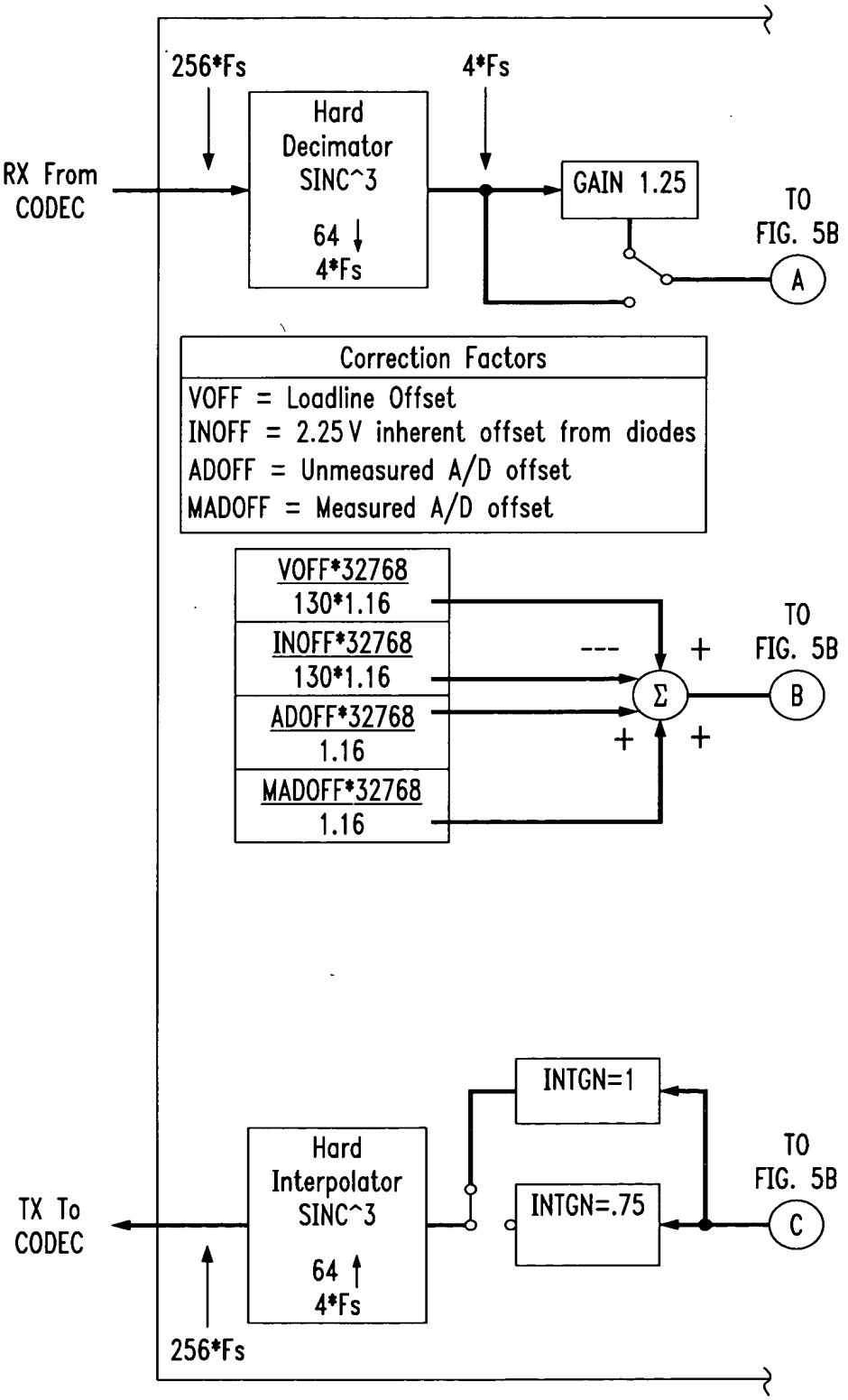


FIG. 5B

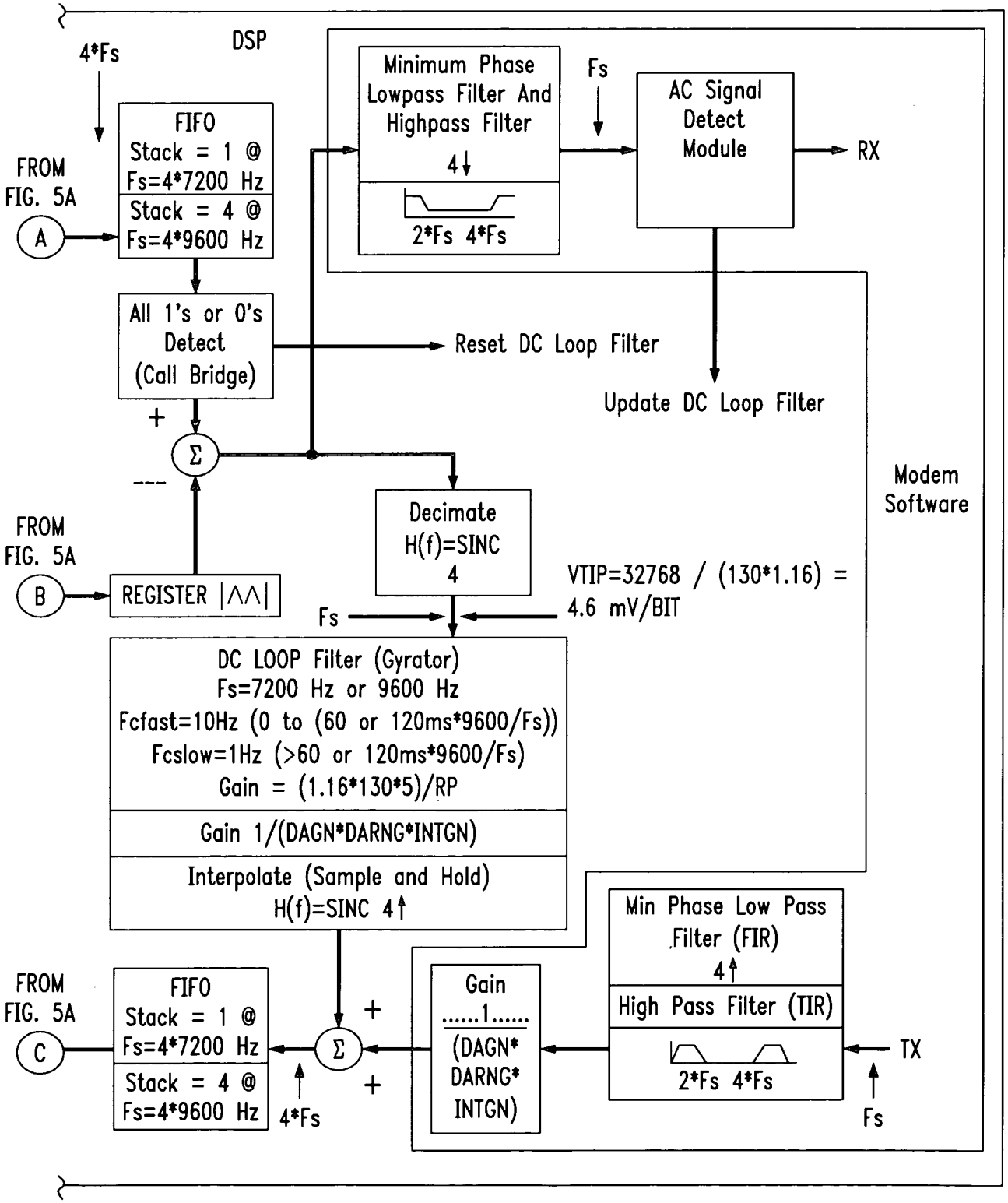


FIG. 6

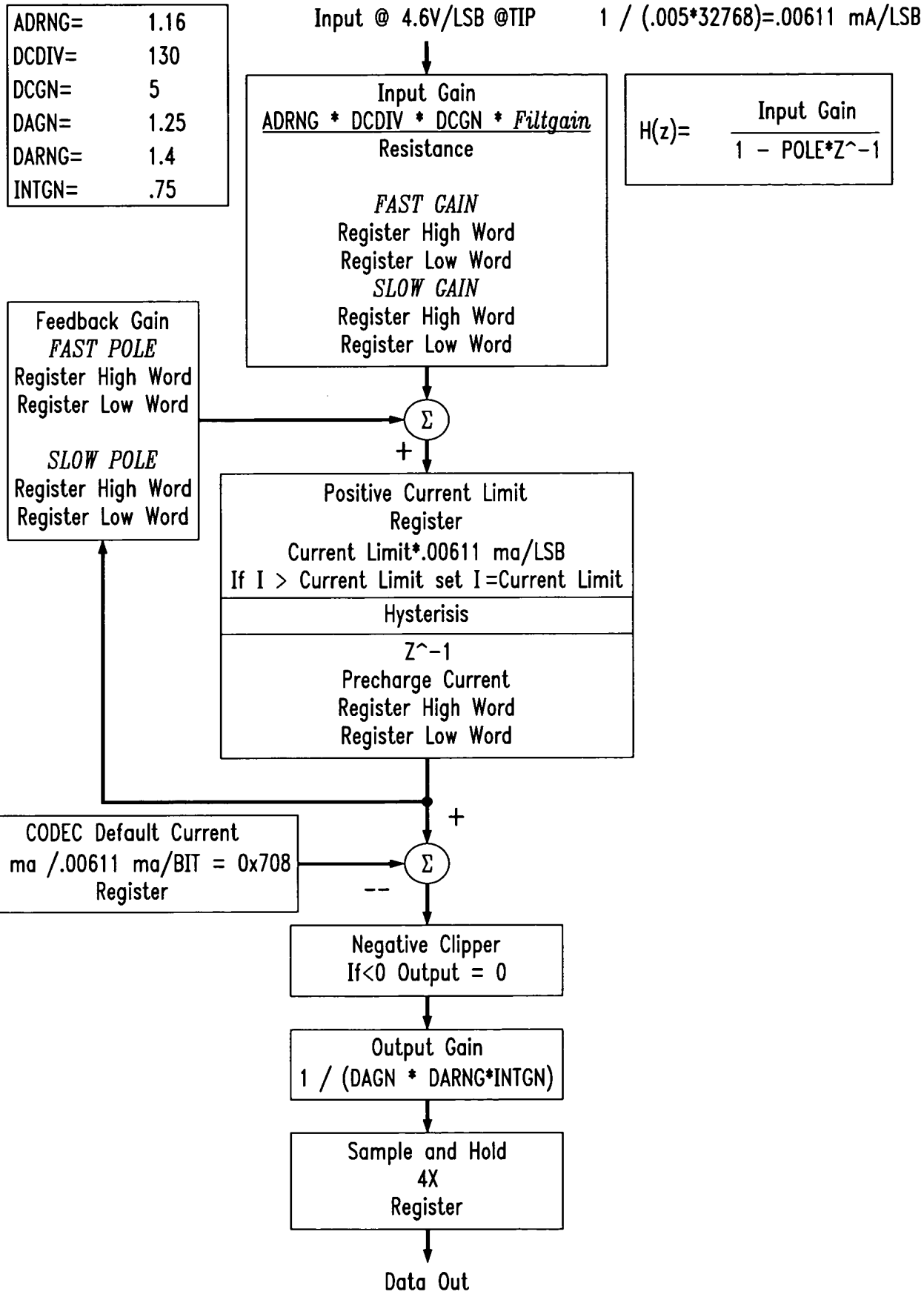


FIG. 7A

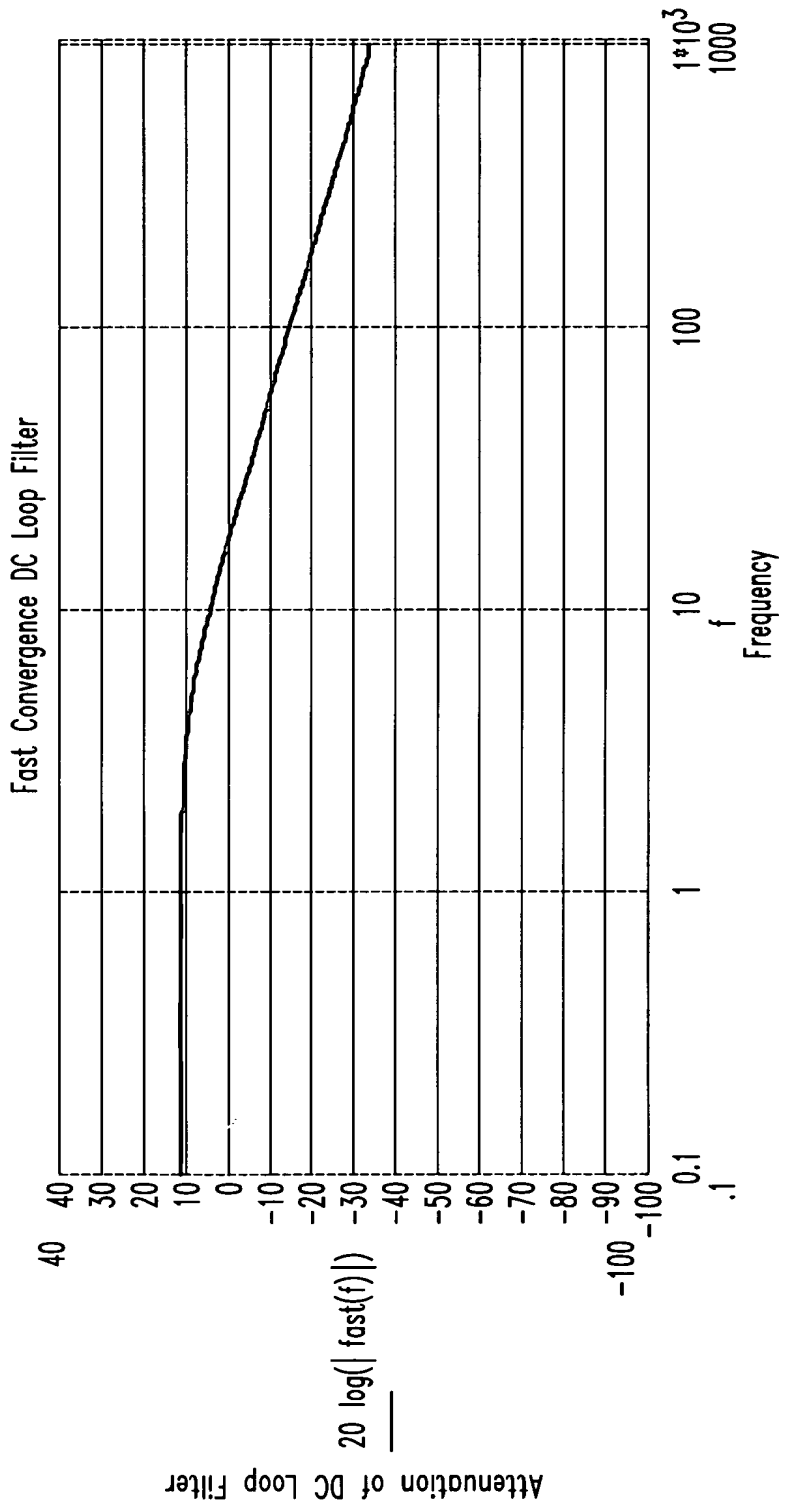


FIG. 7B

10 Hz Fast DC Loop Filter Gain and Phase

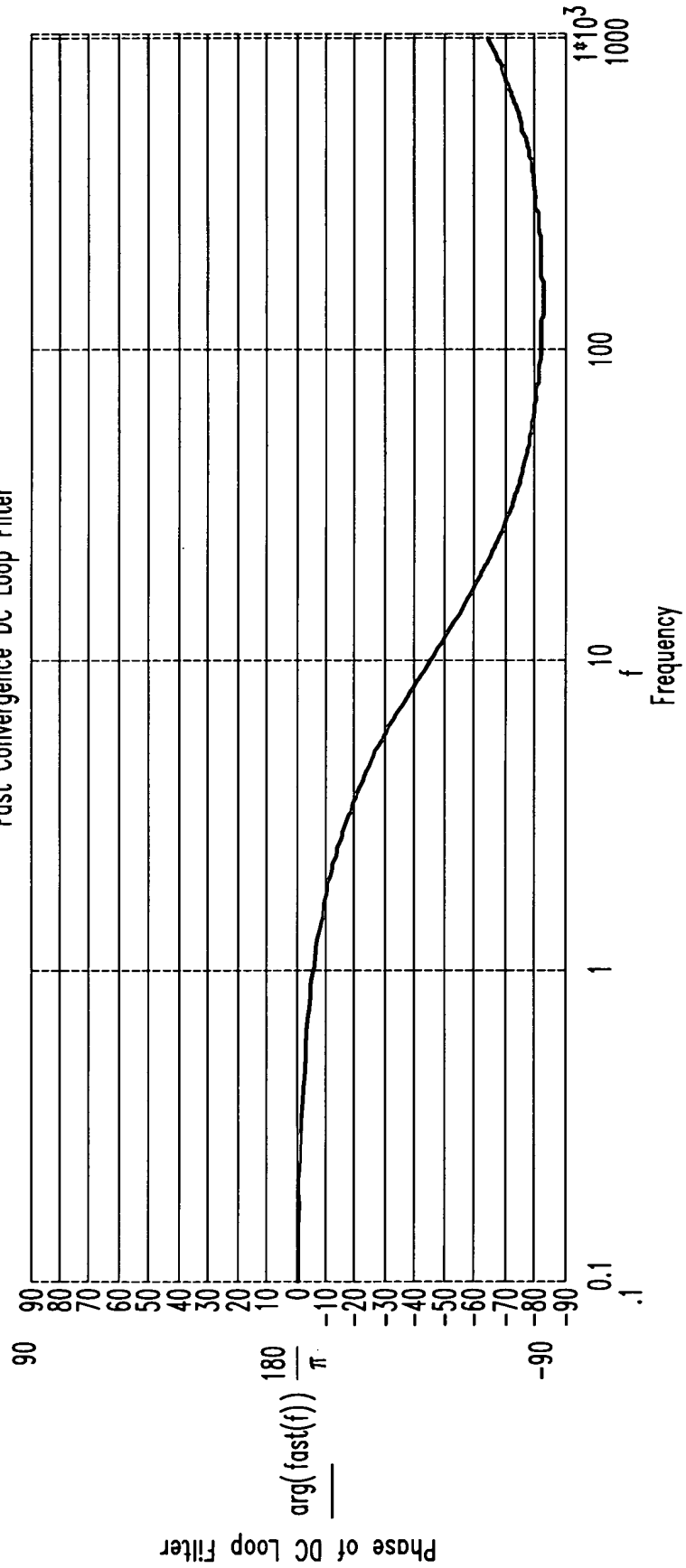


FIG. 8A

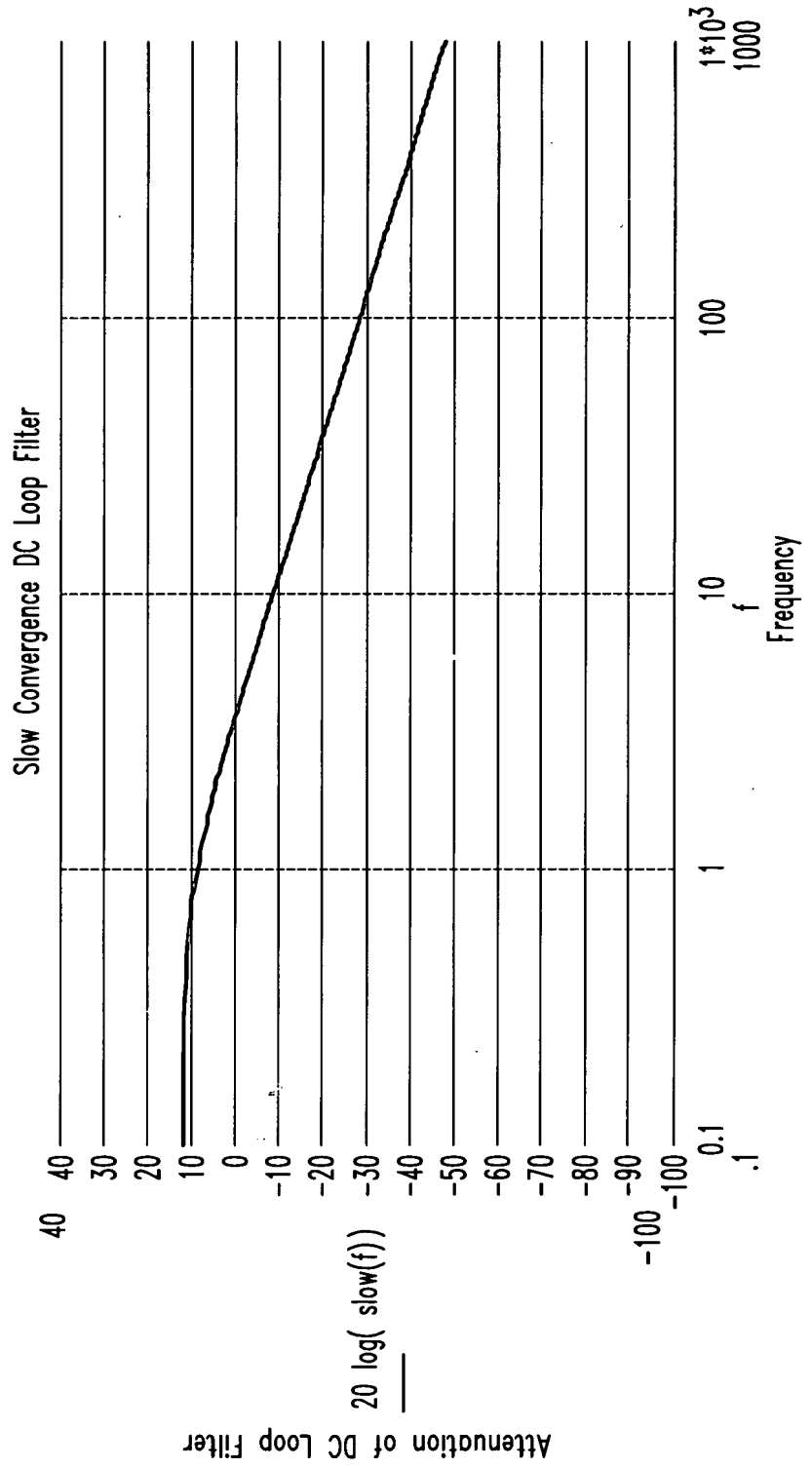


FIG. 8B

1 Hz Slow DC Loop Filter Gain and Phase

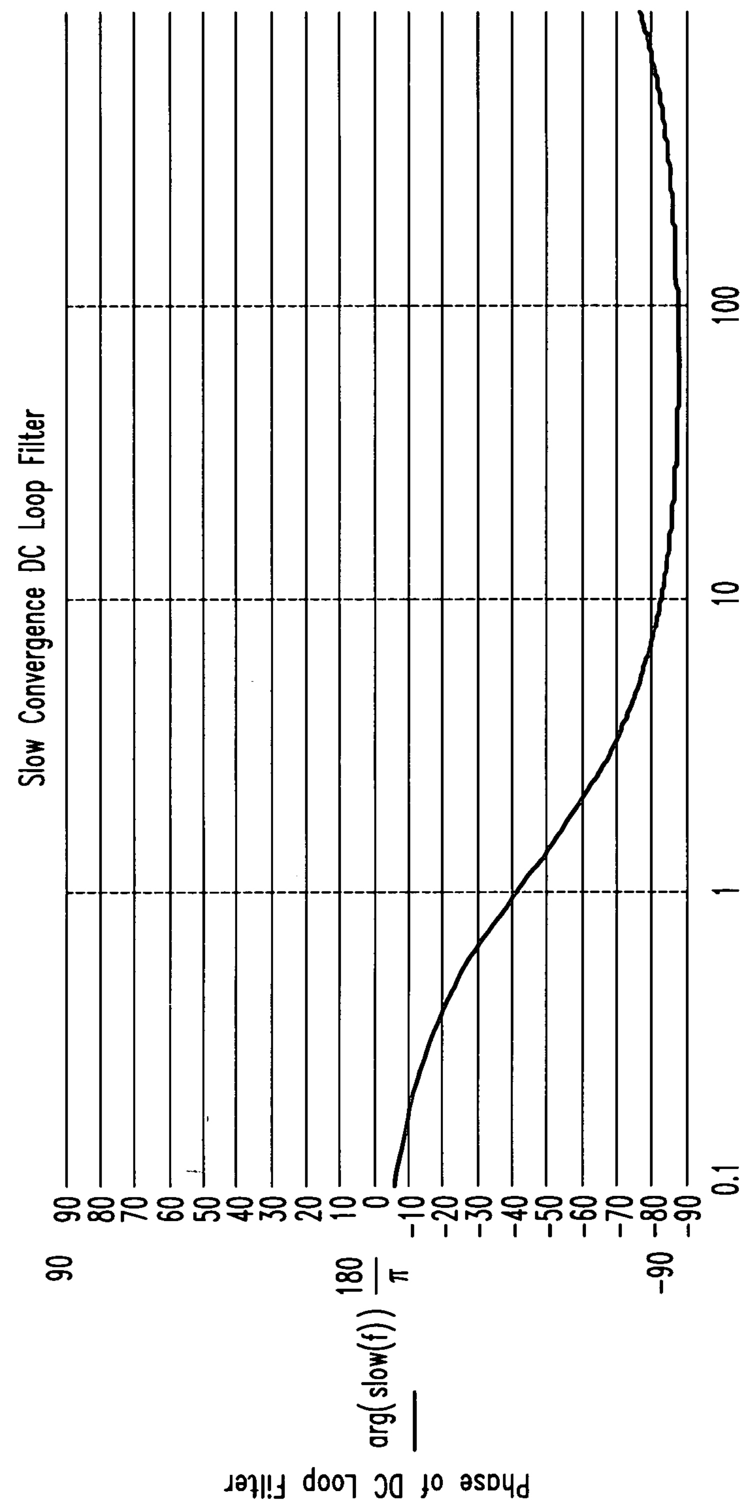


FIG. 9

First Order Filter Topology

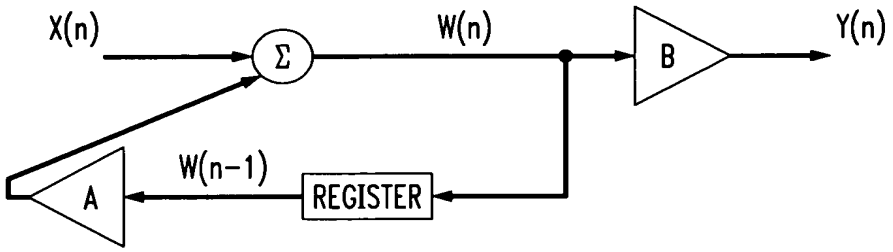
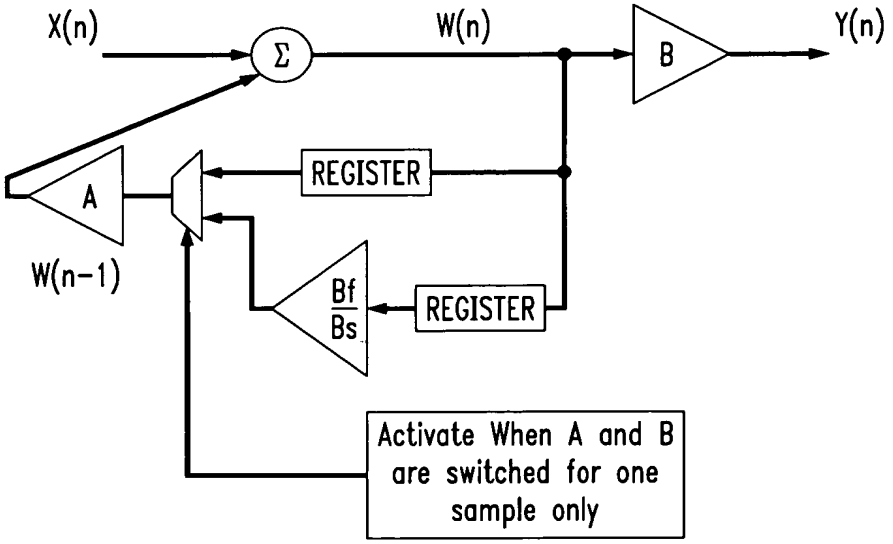


FIG. 10

Final Low Pass Topology with glitch removed



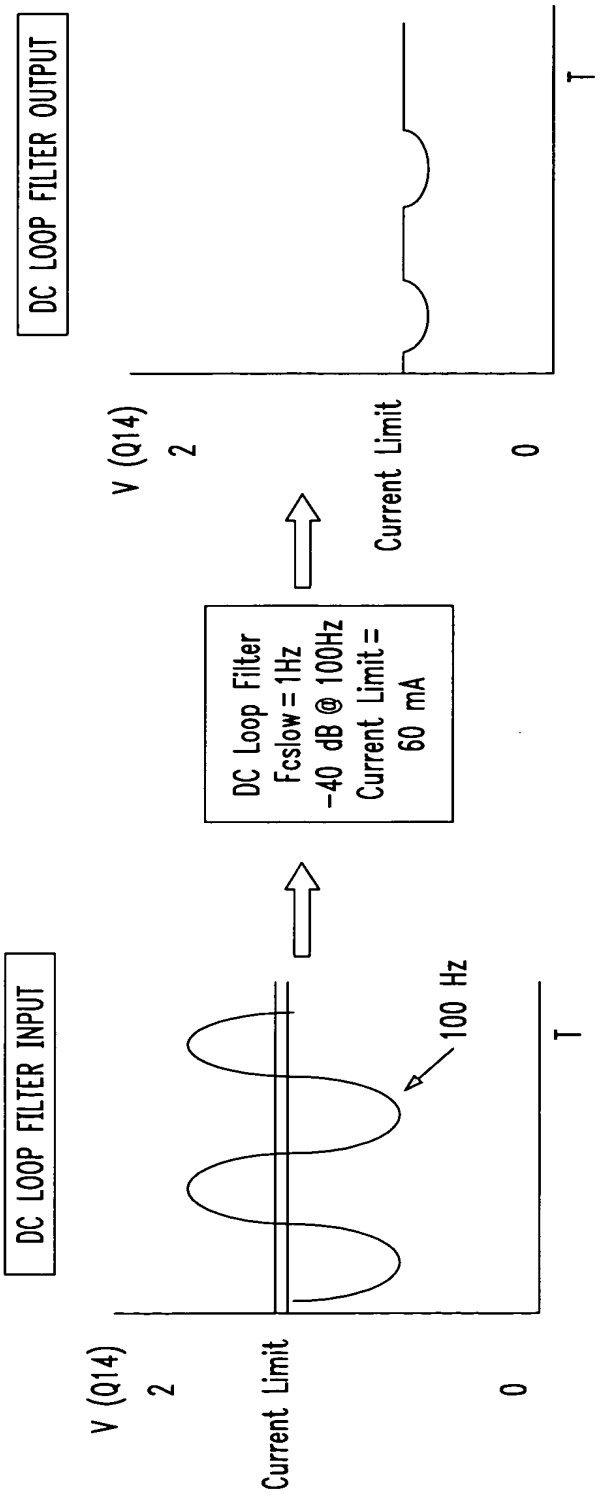


FIG. 11A

DC Loop Filter Without Hysterysis

FIG. 11B

DC Loop Filter With Hysterysis

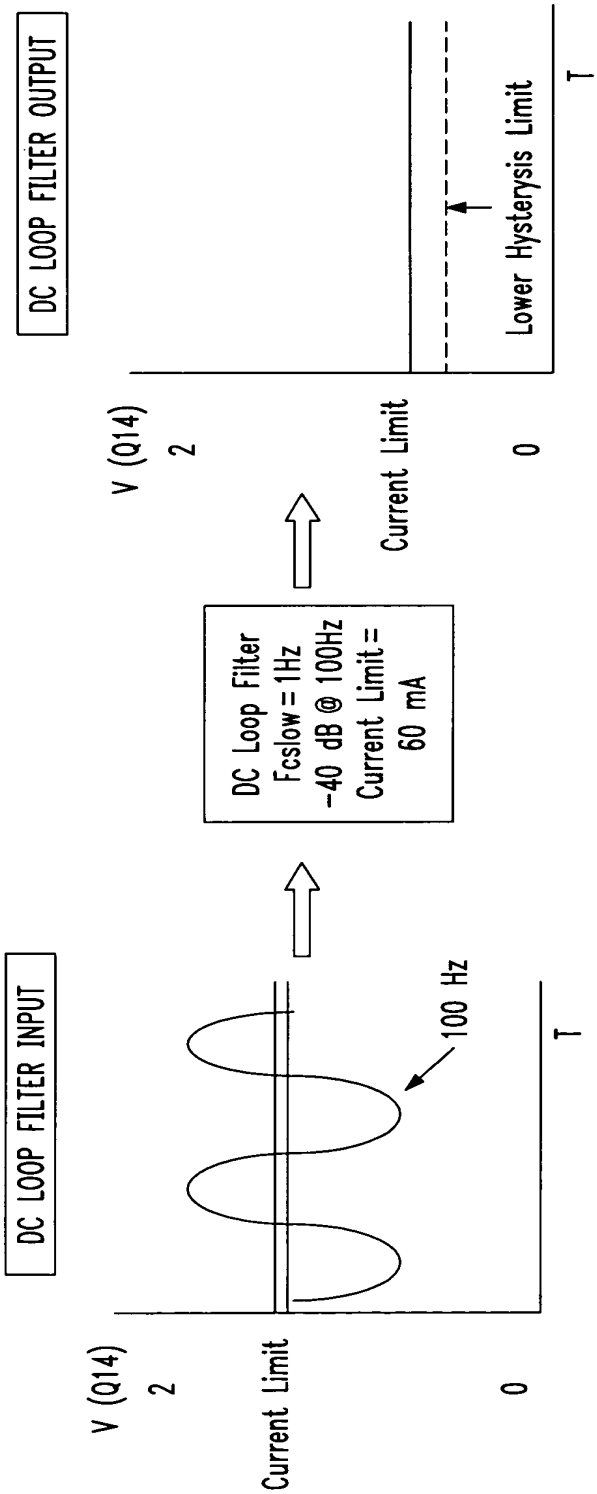


FIG. 12A

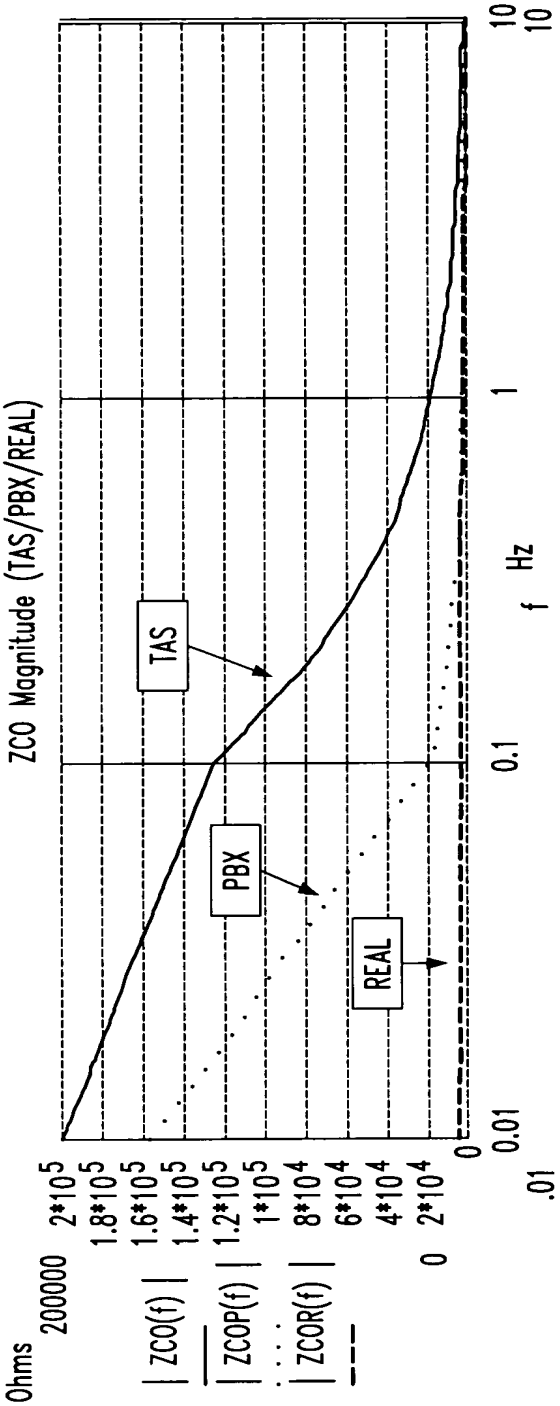


FIG. 12B

TAS, PBX and Real Phone Line V/I Loadlines

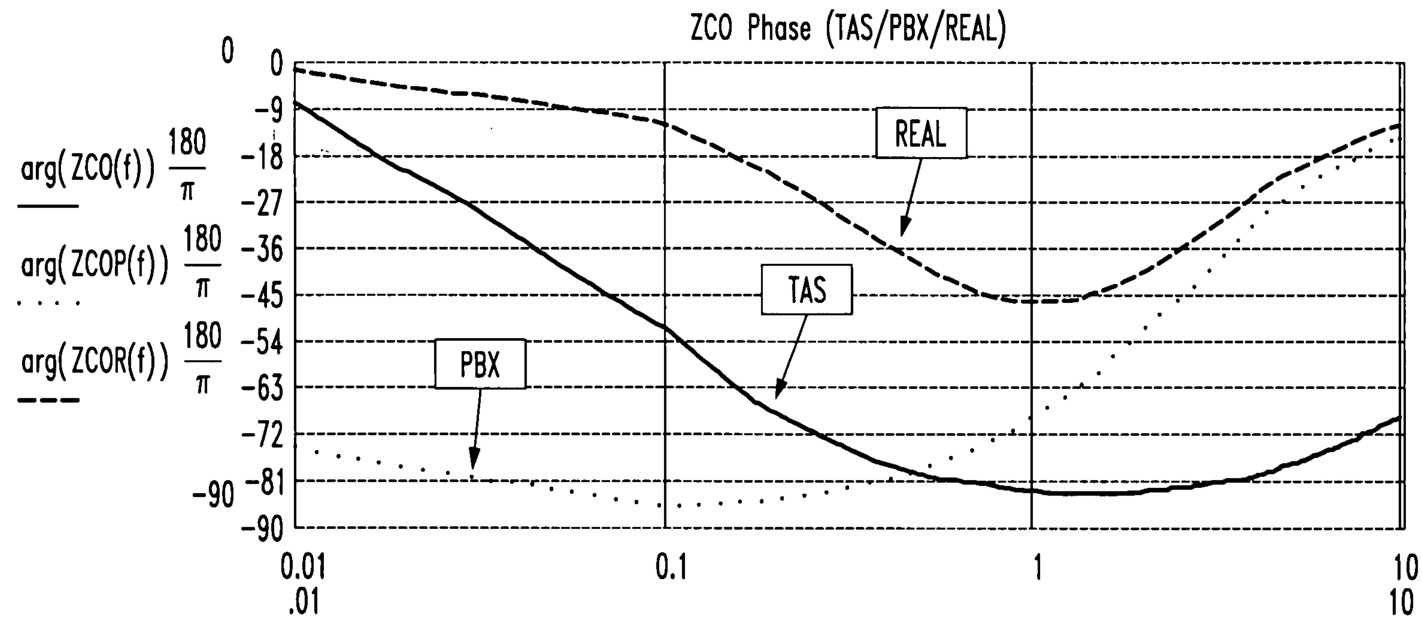


FIG. 13A

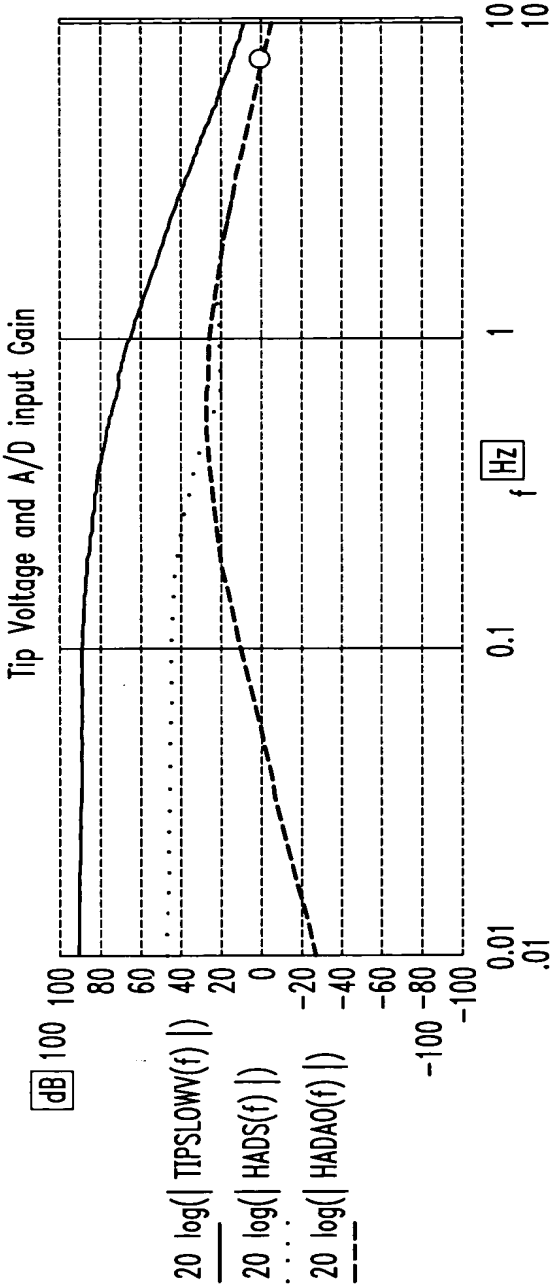


FIG. 13B

TAS Termination with Lowpass Filter Cutoff = 1 Hz

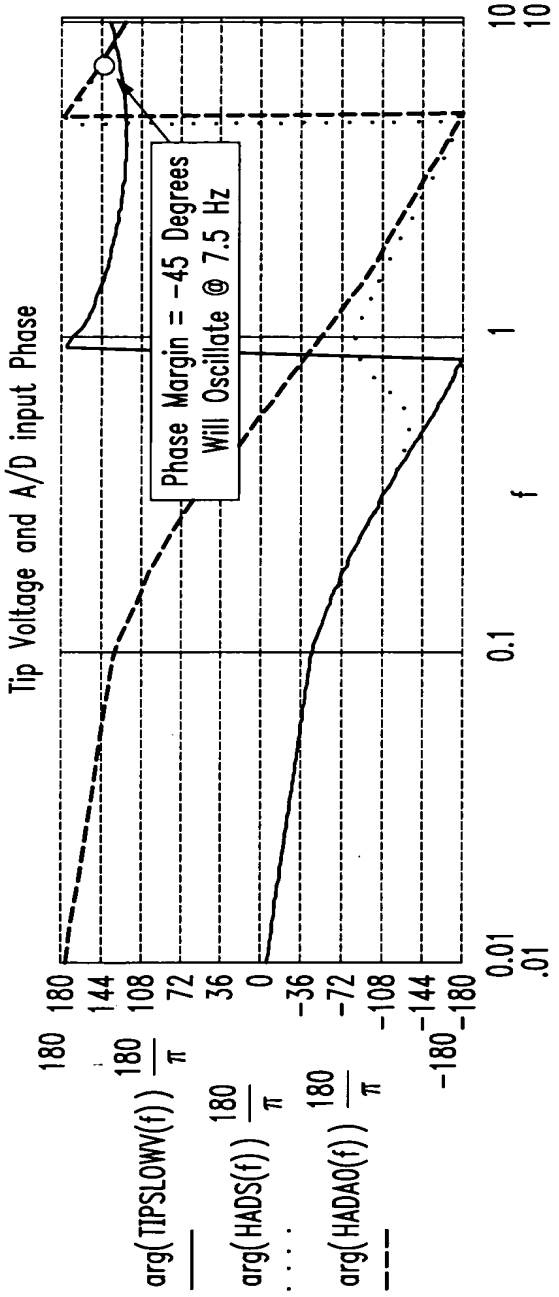


FIG. 14A

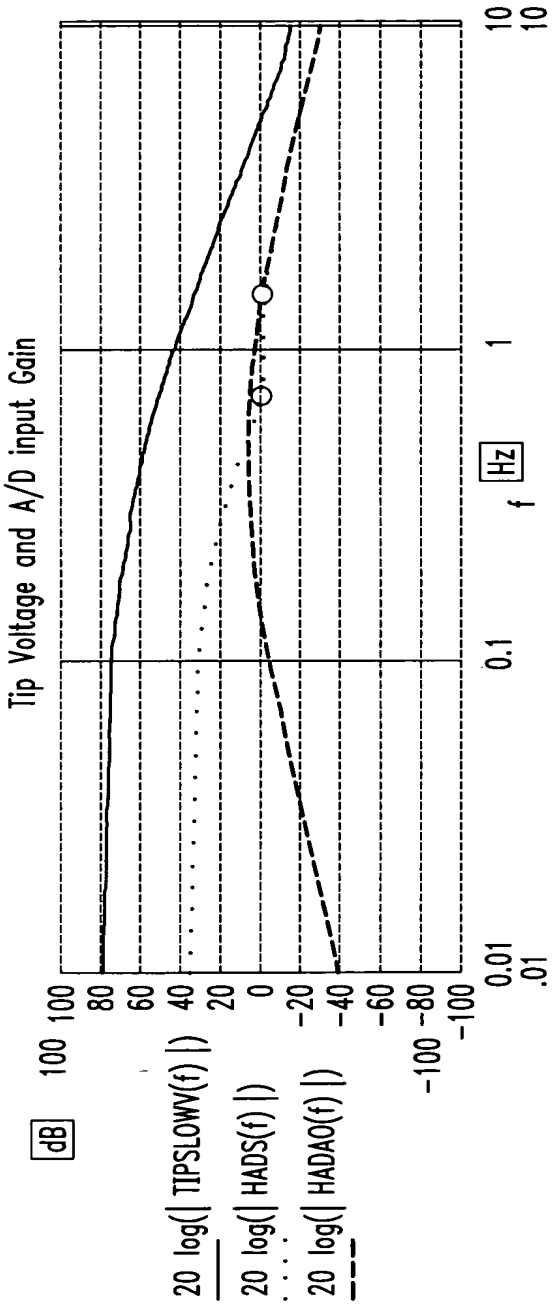


FIG. 14B

TAS Termination with Lowpass Filter Cutoff = .1 Hz

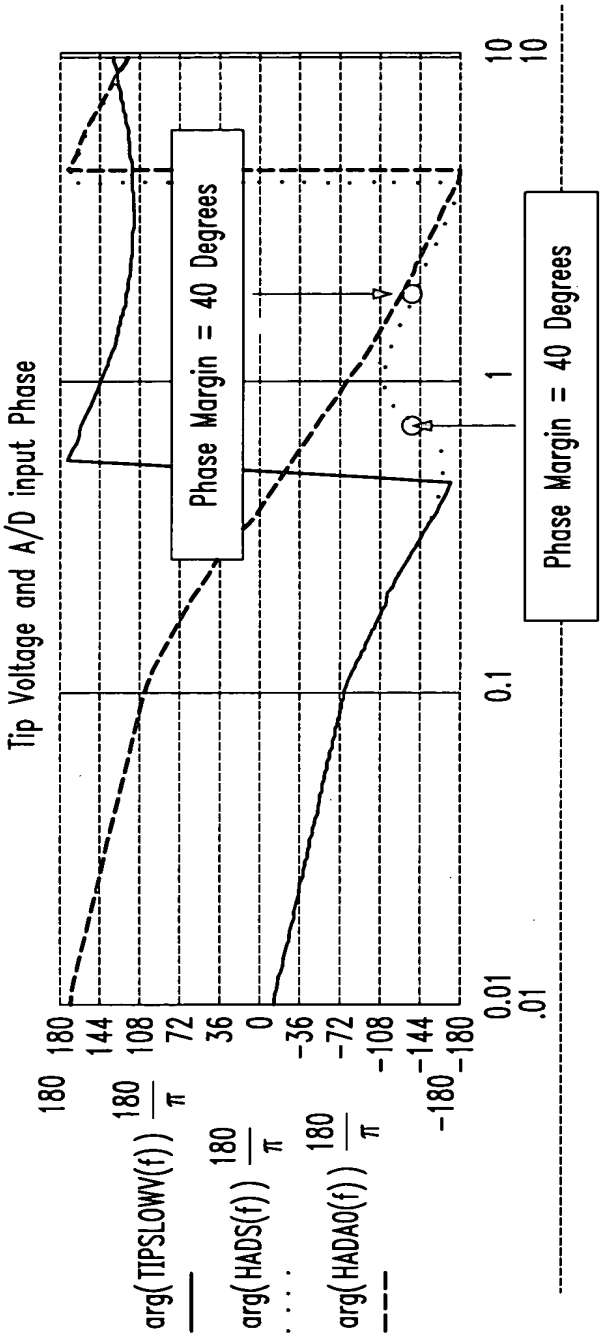


FIG. 15
PRIOR ART

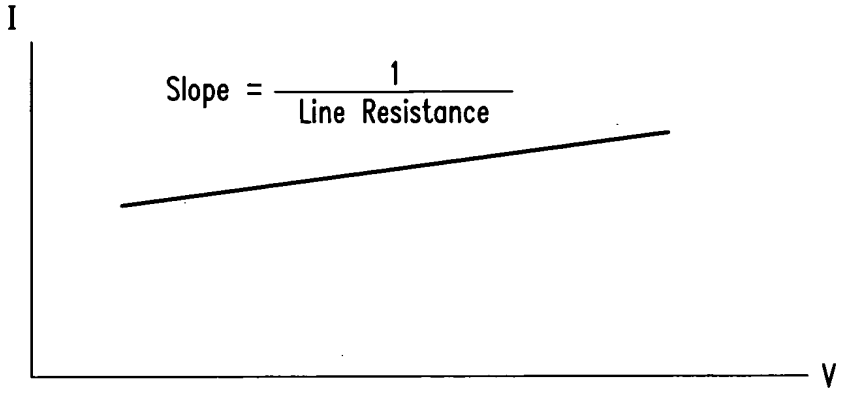


FIG. 16
PRIOR ART

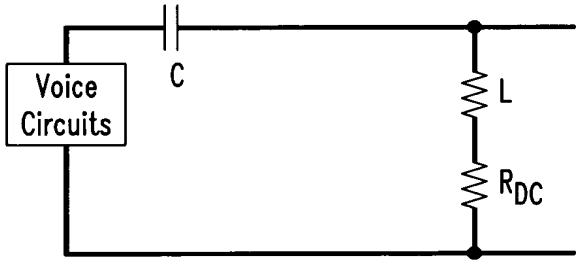


FIG. 17
PRIOR ART

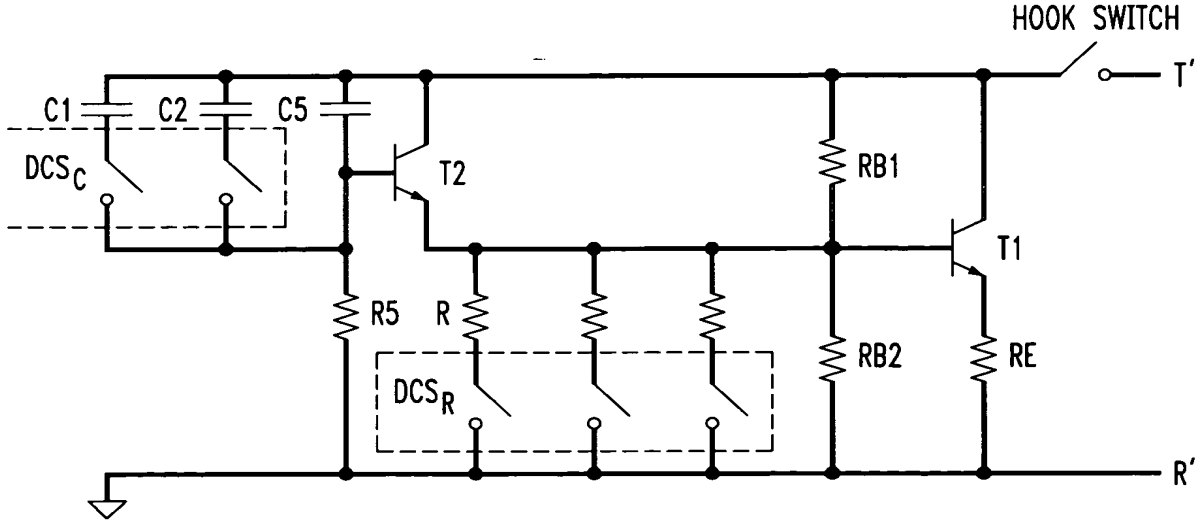
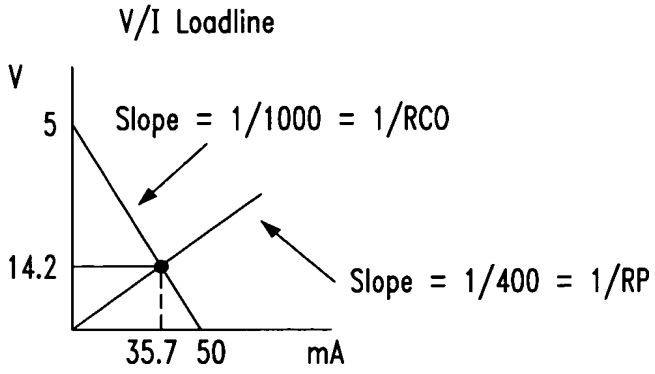


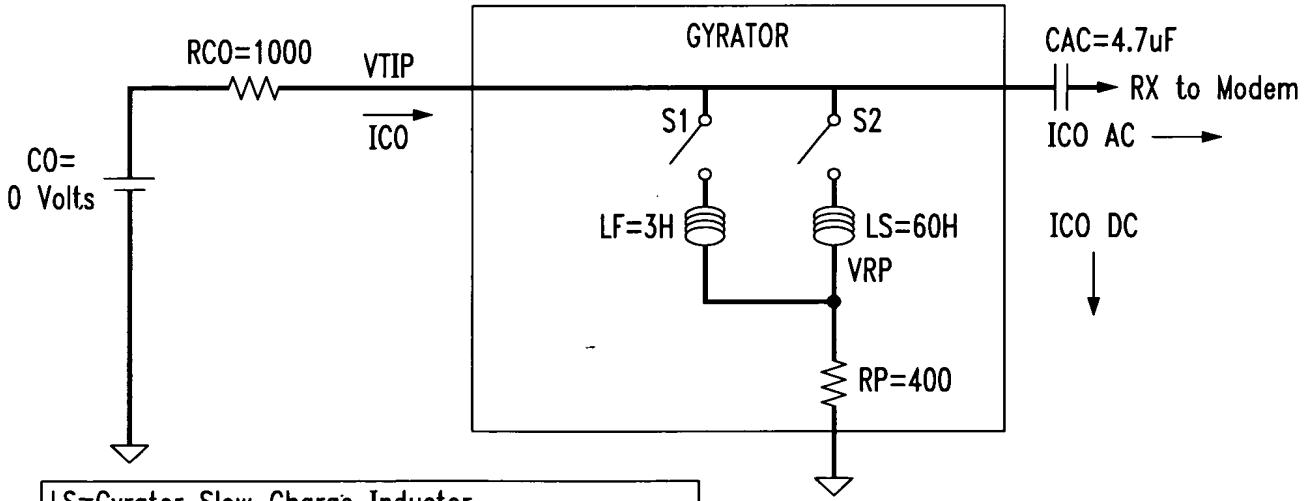
FIG. 18A
PRIOR ART



50-ICO*RCO=ICO*RP=VTIP
ICO=14.27 mA
VP=35.7 Volts
Note: All results are at steady state

FIG. 18B
PRIOR ART

Basic External Gyrator Example



LS=Gyrator Slow Charge Inductor
LF=Gyrator Fast Charge Inductor
RP=Gyrator Impedance
CAC=AC coupling capacitor for AC modem signals
RCO=Central Office Resistance